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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,282	02/25/2002	Andy Glew	42390P11202	7096

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EXAMINER	
TRUONG, BAO Q	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,282	GLEW ET AL.	
	Examiner	Art Unit	
	Bao Q Truong	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,13,16,17 and 20* is/are rejected.

7)☒ Claim(s) *2-7,9-11,14,15,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The instant application having Application No. 10/084,282 has a total of 20 claims pending in the application; there are 3 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration is not presented in the application. Submission of the oath/declaration is required.

Information Disclosure Statement

3. As required by M.P.E.P § 609 (C), the applicant's submission of the Information Disclosure Statements, dated on 11/10/03, 03/03/04, 04/22/04, 04/26/04, 06/21/04, 11/22/04, and 01/10/05, are acknowledged by the examiner; and the cited reference has been considered in the examination of the claims now pending. As required by M.P.E.P § 609 C (2), a copy of the PTO-1449 initialed and dated by the examiner is attached to the instant office action.

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 8, 13, 16-17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Brelsford et al. (U.S. Patent No. 5,230,069).

Referring to claim 1, Brelsford teaches a method comprising:

dividing a physical address space into a plurality of segments as dividing a physical memory space of virtual machine system (see Abstract) into multiple segments (see figure 6; figure 8: element 805; and column 12: lines 19-24);

computing an interim first address from a physical address from the physical address space as adding Main Storage Origin (MSO) value to a guest absolute address (see figure 8: step 810; figure 9B: elements 912 and 914);

computing an interim base value from a base value associated with the physical address as obtaining a main storage extent value associated with the guest virtual machine (see figure 9B element 913);

comparing the interim first address and the interim base value to determine whether the physical address can be validly translated to obtain a translated address as comparing the result of adding the MSO value to the guest absolute address with the effective main storage extent

value to check if the resultant address is valid (see figure 9B: element 915; column 12: lines 34-37 and column 14: lines 17-19); and

if the physical address can be validly translated, combining the physical address with an offset value to obtain the translated address as if the resultant address is valid, it is then used to obtain a corresponding host absolute address (see figures 1 and 3: steps 106-110).

As to claim 8, Brelsford further teaches a step of issuing a fault alert as issuing a host translation exception (interruption) (see figure 10C: step 199-200 and column 11: lines44-47).

Referring to claim 13, Brelsford discloses an apparatus comprising:

a memory having a first address space divided into a plurality of segments as a physical memory space of virtual machine system (see Abstract) divided into multiple segments (see figure 6; figure 8: element 805; and column 12: lines 19-24);

comparison logic circuitry (see figure 9B: combination of elements 912-915) coupled to the memory to create an interim first address from a first address from one of the plurality of segments as adding Main Storage Origin (MSO) value to a guest absolute address (see figure 8: step 810; figure 9B: elements 912 and 914), to create an interim base value as obtaining a main storage extent value associated with the guest virtual machine (see figure 9B element 913), and to compare the interim first address and the interim base value to determine whether the first address belongs to a segment that can be validly translated to obtain a second address as comparing the result of adding the MSO value to the guest absolute address with the effective

main storage extent value to check if the resultant address is valid (see figure 9B: element 915; column 12: lines 34-37 and column 14: lines 17-19); and

combination logic circuitry coupled to the comparison logic circuitry and to the memory, the combination logic circuitry to combine the first address with an offset value to obtain the second address if the comparison logic circuitry indicates that the first address can be validly translated as if the resultant address is valid, a host dynamic-address-translation (DAT) used the resultant address to obtain a corresponding host absolute address (see figures 1 and 3: steps 106-110 and see figure 9B: element 905).

As to claim 16, Brelsford further discloses a fault detection circuitry coupled to the comparison logic circuitry, the fault detection circuitry to detect and issue fault alerts as issuing a host translation exception (interruption) (see figure 10C: step 199-200 and column 11: lines44-47).

Referring to claim 17, Brelsford discloses a system comprising:

a processor as inherently exists in a virtual machine computer system (see Abstract);

memory coupled to the processor, the memory having a first address space divided into a plurality of segments as a physical memory space of virtual machine system (see Abstract) divided into multiple segments (see figure 6; figure 8: element 805; and column 12: lines 19-24);

comparison logic circuitry (see figure 9B: combination of elements 912-915) coupled to the memory to create an interim first address from a first address from one of the plurality of segments as adding Main Storage Origin (MSO) value to a guest absolute address (see figure 8:

step 810; figure 9B: elements 912 and 914), to create an interim base value as obtaining a main storage extent value associated with the guest virtual machine (see figure 9B element 913), and to compare the interim first address and the interim base value to determine whether the first address belongs to a segment that can be validly translated to obtain a second address as comparing the result of adding the MSO value to the guest absolute address with the effective main storage extent value to check if the resultant address is valid (see figure 9B: element 915; column 12: lines 34-37 and column 14: lines 17-19); and

combination logic circuitry coupled to the comparison logic circuitry and to the memory, the combination logic circuitry to combine the first address with an offset value to obtain the second address if the comparison logic circuitry indicates that the first address can be validly translated as if the resultant address is valid, a host dynamic-address-translation (DAT) used the resultant address to obtain a corresponding host absolute address (see figures 1 and 3: steps 106-110 and see figure 9B: element 905).

As to claim 20, Brelsford further discloses a fault detection circuitry coupled to the comparison logic circuitry, the fault detection circuitry to detect and issue fault alerts as issuing a host translation exception (interruption) (see figure 10C: step 199-200 and column 11: lines44-47).

Allowable Subject Matter

7. Claims 2-7, 9-11, 14-15, and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (571) 272-4202. The examiner can normally be reached on Monday-Friday from 6:00 AM to 3:00 PM (ET).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

BAO QUOC TRUONG

BT

Patent Examiner

01 June 2005

Donald Sparks

Supervisory Patent Examiner

Technology Center 2100